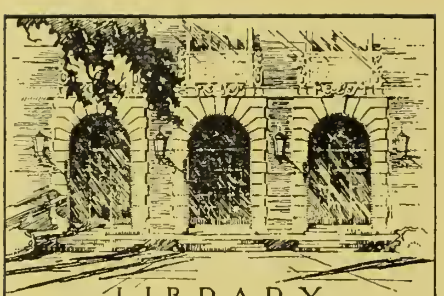

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REPORT NO. 152

PERFORMANCE CHARACTERISTICS OF FAST LOGIC FOR ILLIAC III: BASIC NAND AND NOR CIRCUITS

by

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1. GENERAL ASPECTS

For the basic logic circuit of the computer, many possible circuit configurations giving 15 mc to 20 mc operation, could be proposed. For instance, nonsaturated current-steering logic, or again, conventional saturated transistor diode logic with a selection of diode, resistance, or capacitance resistance coupling could be used. That is, the critical speed range of 10 mc to 20 mc can be accomplished either by saturated or low-level unsaturated transistor circuitry.

From the standpoint of economy, saturated logic circuitry is cheaper, simpler and also more stable in the presence of noise and supply voltage variations. However, to overcome the storage delay of saturated logic, we must sacrifice some logical gain; this disadvantage can be minimized by the use of a transistor with a controlled storage time and by proper circuit design. For example the silicon transistor 2N2369 is one device particularly well suited to saturated logic. Using this transistor with high-speed switching diodes, we can expect a propagation delay of less than 20 nsec per stage of logic.

From the standpoint of circuit performance, the NAND circuit is preferable (for silicon devices). Reasons include:

1. All output stages from one preceding stage are independent for the NAND, but not independent for the NOR.
2. Voltage characteristics of the level-shifting diodes, particularly those connected to the same input, must be more uniform in the NOR circuit.
3. In the NAND circuit, fanout with a specified propagation delay is limited mainly by the amount of parasitic capacitance; but in the NOR circuit, both by capacitances and by I_C.
4. For the NAND, propagation delay is relatively independent of the number of fanouts if capacitance is kept small and the circuit designed properly. This results from the small turn-on time variation with the number of fanouts and the fast turn-off characteristics[1] of the NAND circuit.

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[1] See Appendix B.

The short turn-on time is a result of speed compensation of the transistor characteristics[1] by means of the

$$\frac{\partial h_{FE}}{\partial I_C} > 0$$

for I_C in the range of 10 ma to 40 ma.

5. From the point of view of gate driver applications, the NAND gate driver is superior both in signal quality and power consumption.

These features have been investigated in the experiment report below.

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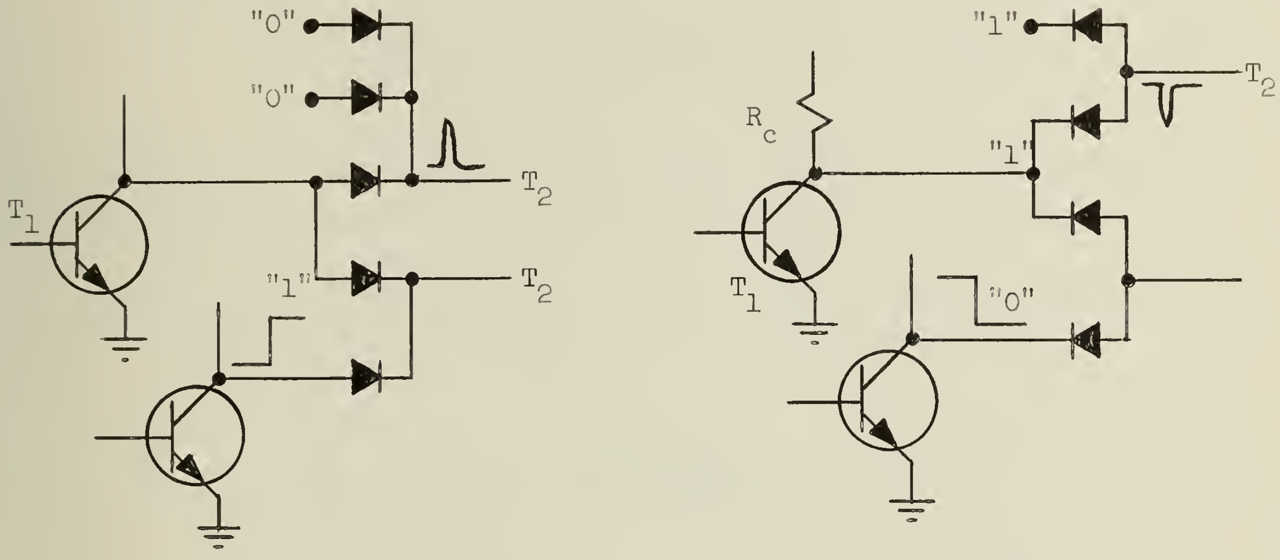
[1] See Appendix A.

2. THE NOISE PROBLEM

The noise problem is different for the NAND and the NOR circuit. Logic noise (spikes) which can disturb the logic operation of the circuit in the following situations:



(a) NOR (b) NAND

Figure 1

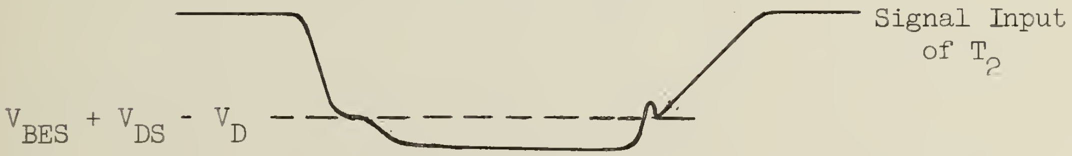


Figure 2

Allowable maximum slow noise signal $V_{N(max)}$ of NAND circuit is

$$V_{N(max)} = V_{CL} - (V_{BE(sat)} + V_{DS} - V_D) \tag{2.1}$$

and that of NOR circuit is given by

$$V_{N(max)} = V_{BE(sat)} + V_{DS} + V_D - V_{CE(sat)} \tag{2.2}$$

Here subscript "D" designates the logic diode, "DS" the level-shifting diode; and conventional transistor subscripts will be used throughout.

For high-frequency noise, the input circuit transfer function of the NAND circuit (Fig. 3) is approximated by the following equation:

$$\frac{p^2 R_C C_D^2 r_B}{(1 + pC_D E_C)[1 + pC_D(r_{DS} + r_B)]} \tag{2.3}$$

(nonclamped case)

where

r_{DS} = ac resistance of level-shifting diode in the conducting region

r_B = ac-base resistance of the transistor in the conducting region

C_D = logic diode junction capacitance

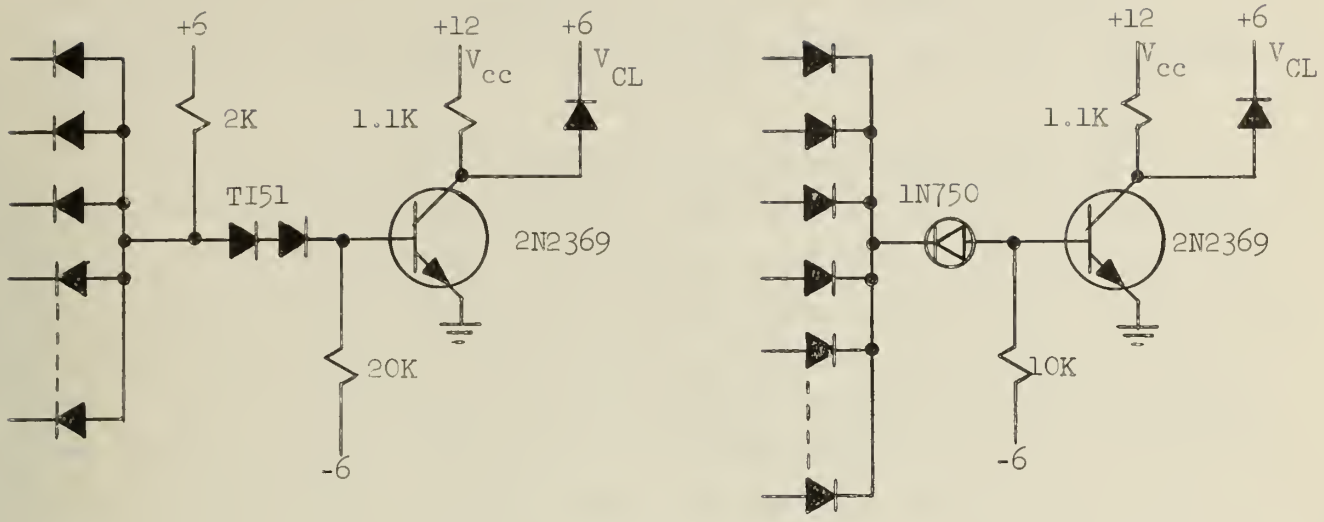
R_C = collector load resistance

p = Laplace transform frequency operator

For the clamped case, capacitance of the level-shifting diode and equivalent capacitance of the base contribute very little:

$$\frac{p^2 r_{CL} C_D^2 r_B}{1 + pC_D(r_{DS} + r_B)} \tag{2.4}$$

(clamped case)



(a) NAND

(b) NOR

Figure 3

Here r_{CL} is the ac resistance of the clamping diode in the conducting region. Therefore r_{CL} is very small. The clamping diode is very important in decreasing noise. A small margin for noise will be assigned for $V_{BE(sat)}$ in the design.

The NOR circuit is designed with an eye for turn-off speed to give logic and level shifting diode disconnection when T_2 is in the off state (see Fig. 3). Therefore the transfer equation is given by

$$\frac{p^2 R_B r_C C_D C}{1 + R_B pC} \qquad (2.5)$$

where

C = resultant capacitance of the logic diode and level-shifting diode

R_B = base bias resistance

$r_C = \frac{\partial V_{CE}}{\partial I_C}$ at the designated I_C value. This value is roughly equal to twice r_D.

The noise transfer equation is of the same form as in the clamped NAND circuit, but r_C, R_B are greater than r_{CL}, r_B. Therefore, logic noise in the NOR circuit can be expected to be somewhat greater than noise in the NAND circuit.

For an npn silicon transistor, the positive NAND logic circuit is preferable to the NOR circuit. In some cases, for instance, for a decoder the NOR circuit is more economical. Consequently some NAND circuits can have NOR circuit loads, and some NOR circuits can have NAND circuit loads. Actually the collector clamping diode is not necessary in the NOR circuit, if the load is always a NOR circuit, but when the load contains a NAND circuit, the clamping diode of the NOR circuit increases circuit speed and decreases noise in the following NAND circuit. For this reason the basic NOR circuit has a collector clamping diode as does the NAND circuit.

In this report the performance characteristics of the basic logic circuits are reported with test data taken from prototype printed-circuit boards. Design and operating speed consideration are given in the two appendices. In high-speed operation, the printed-circuit board is as important as the design of the circuit as is the parameter specification of the transistor.

3. BASIC PERFORMANCE CHARACTERISTICS

The basic characteristics of the circuit in Figs. 3a and 3b are shown in Figs. 4a and 4b and Figs. 5a and 5b respectively.

Figure 4 shows the dc operating range, and Fig. 5 shows the basic speed data. Data in Figs. 4 and 5 were not taken from a circuit on a test printed-circuit board but rather from a separately-fabricated circuit having no fanout.

Figure 5 shows the effect of the capacitive feedback between collector and base, and the effect of the output capacitance. These results provide a reference point to discuss the performance of the circuit on the printed board used for test purposes (see below).

Figure 6 shows the effect of the wiring on the board. The output capacitance causes a slow turn-off time, but does not affect the turn-on time. The negative feedback through collector-to-base capacitance slows down both turn-on and turn-off speed. The coupling between collector and base conductors, if they are long, must be watched carefully. Too much coupling here causes the propagation delay to become too large. In the NAND circuit propagation delay depends more upon turn-on speed than the turn-off speed.[1]

Figure 7 shows the effect of the fanout on both turn-on and turn-off time. When the number of fanouts is increased, output capacitance increases linearly.

Therefore, turn-off time increases in direct proportion to the number of fanouts. Turn-on time does not depend much on the number of fanouts but in a properly designed circuit, turn-off time doesn't contribute to the propagation delay. On the other hand, turn-on time contributes to the delay but when we select the transistor to have the characteristics of

$$\frac{\partial h_{FE}}{\partial I_C} > 0$$

as explained before, in the region of important range of I_C, turn-on time does not change appreciably until the number of fanout reaches about ten. On the

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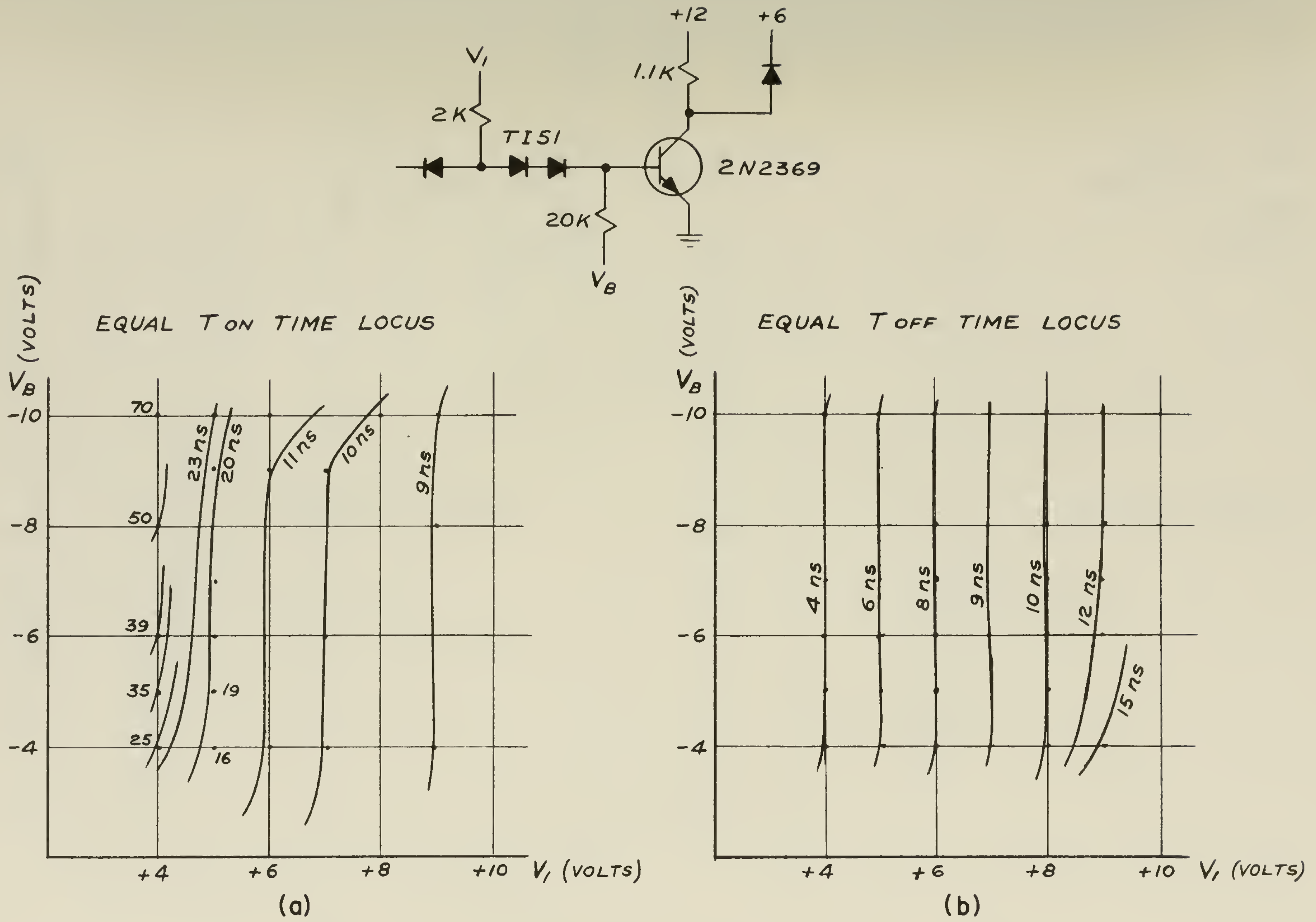
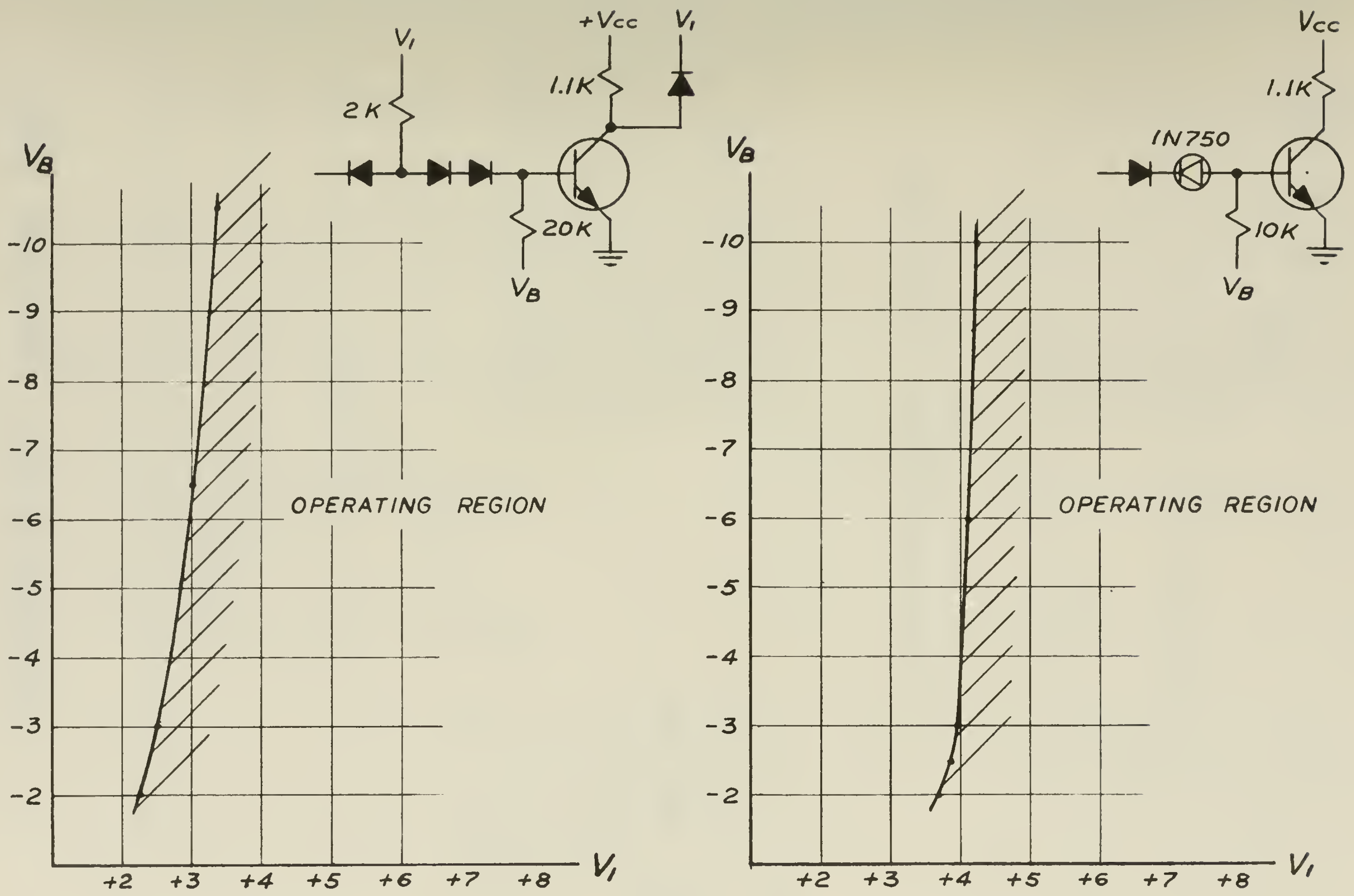
[1] See Appendix 2.



SWITCHING CHARACTERISTICS
OF THE NAND CIRCUIT

FIGURE 4.

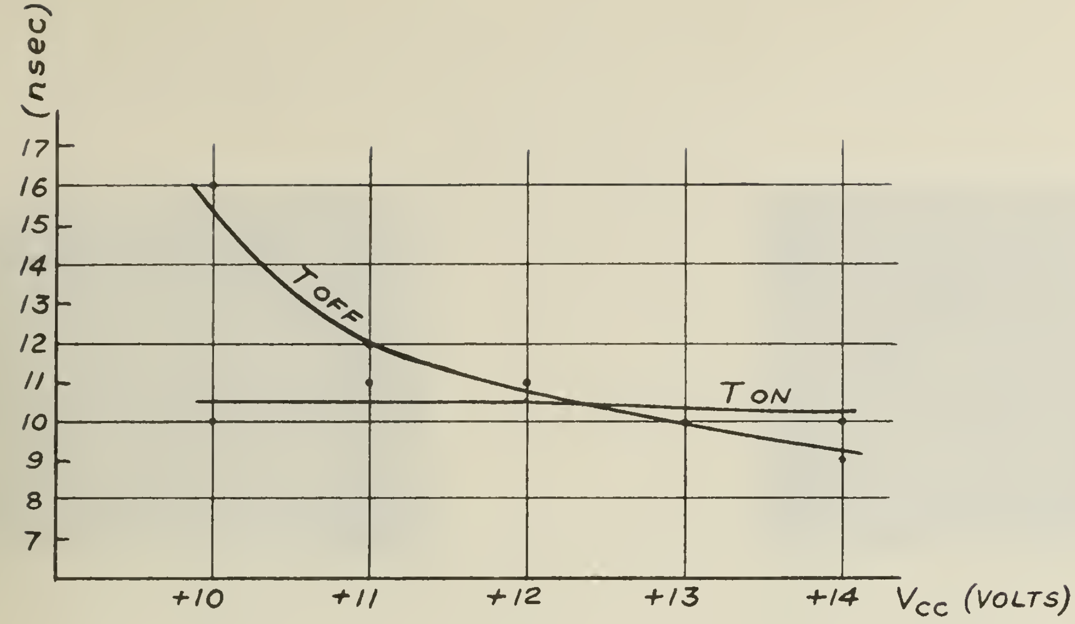


(a')
NAND

(b')
NOR

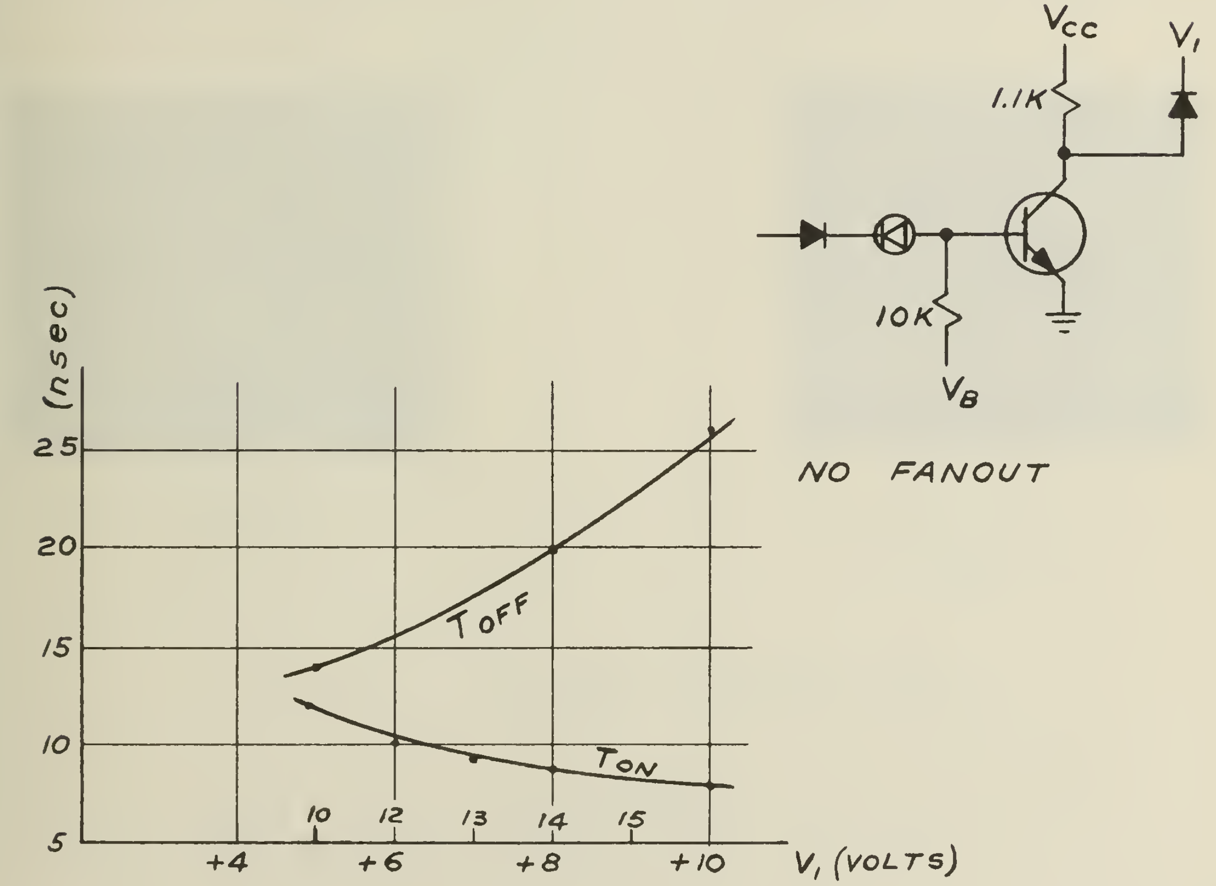
OPERATING BOUNDARY

FIGURE 4.



(c)

SWITCHING CHARACTERISTICS vs V_{CC}



(d)

BASIC SWITCHING CHARACTERISTICS

FIGURE 4.

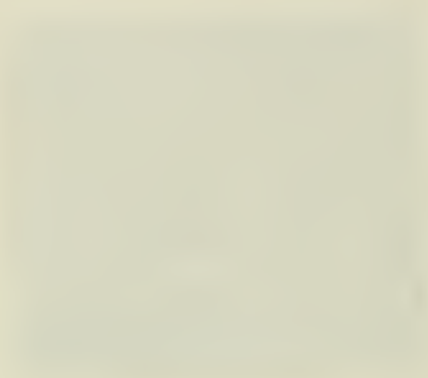
(a) 10 nsec/div
t_{on} 10 nsec

(b) 10 nsec/div
3 pf added between
base and collector

(c) 10 nsec/div
t_{off} 11 nsec

(d) 10 nsec/div
5 pf added to
collector

Figure 5. Basic NAND, isolated fabrication



(a)

(b)

Figure 6. Basic NAND. Same circuit as Fig. 5, but fabricated on a printed-circuit board.

(a) t_{on} waveform with 0 to 6 fanout, R_C = 1.1 K

(b) t_{on} waveform with 0 to 6 fanout, R_C = 560 ohms

(c) t_{off} waveform with 0 to 6 fanout, R_C = 1.1 K, with clamp

(d) t_{off} waveform with 0 to 6 fanout, R_C = 560 ohms, with clamp

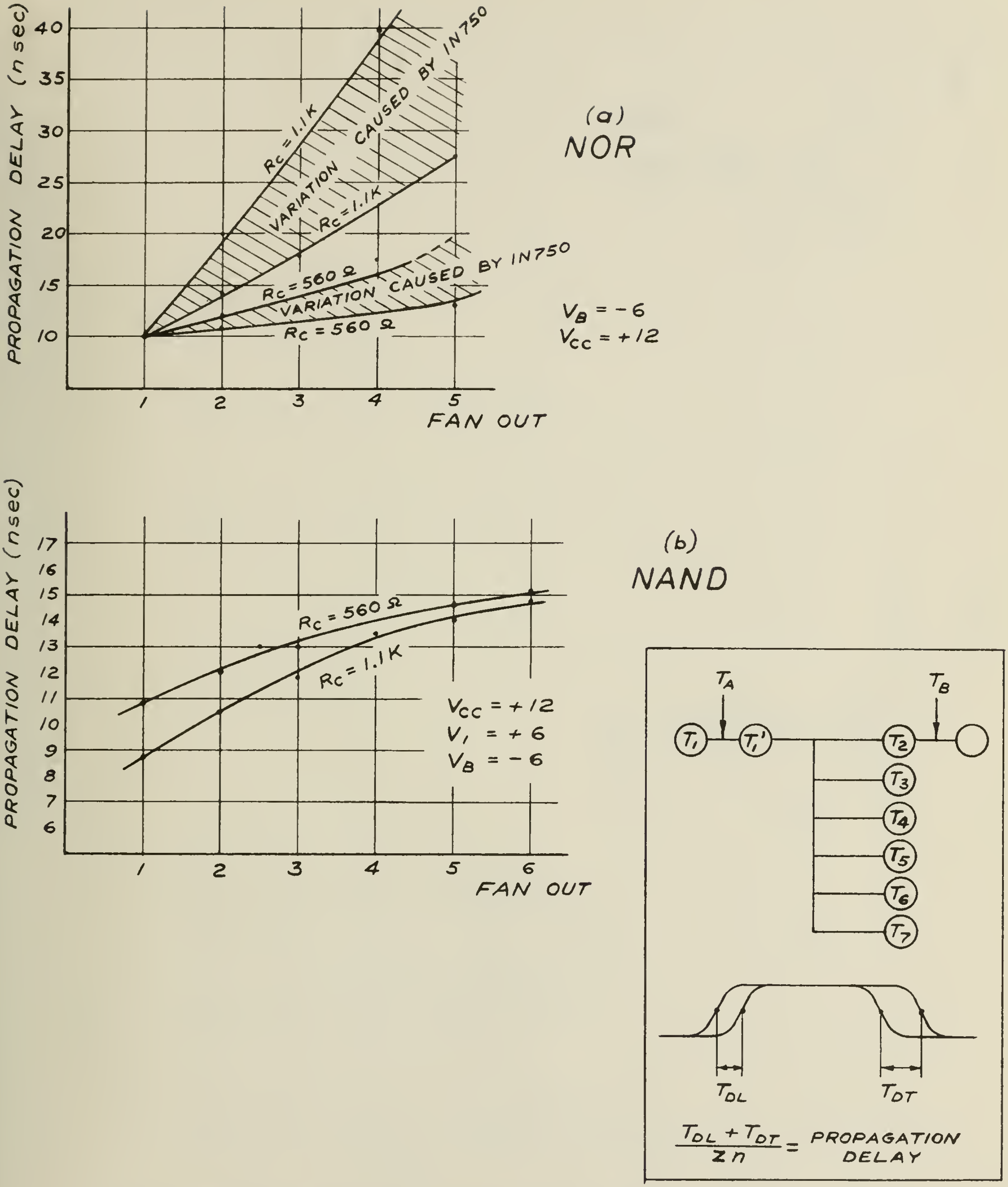
Figure 7

contrary, in the NOR circuit, delay depends more on the turn-off time, and turn-off time increases directly proportional to the number of fanout.

Figure 8 shows the propagation delay versus fanout for both the NAND and the NOR circuit.

Figure 9 shows how propagation delay depends on the values of R_c and V_{cc}.

Figure 10 shows how propagation delay varies with supply voltage.



PROPAGATION DELAY VERSUS FAN OUT

FIGURE 8.

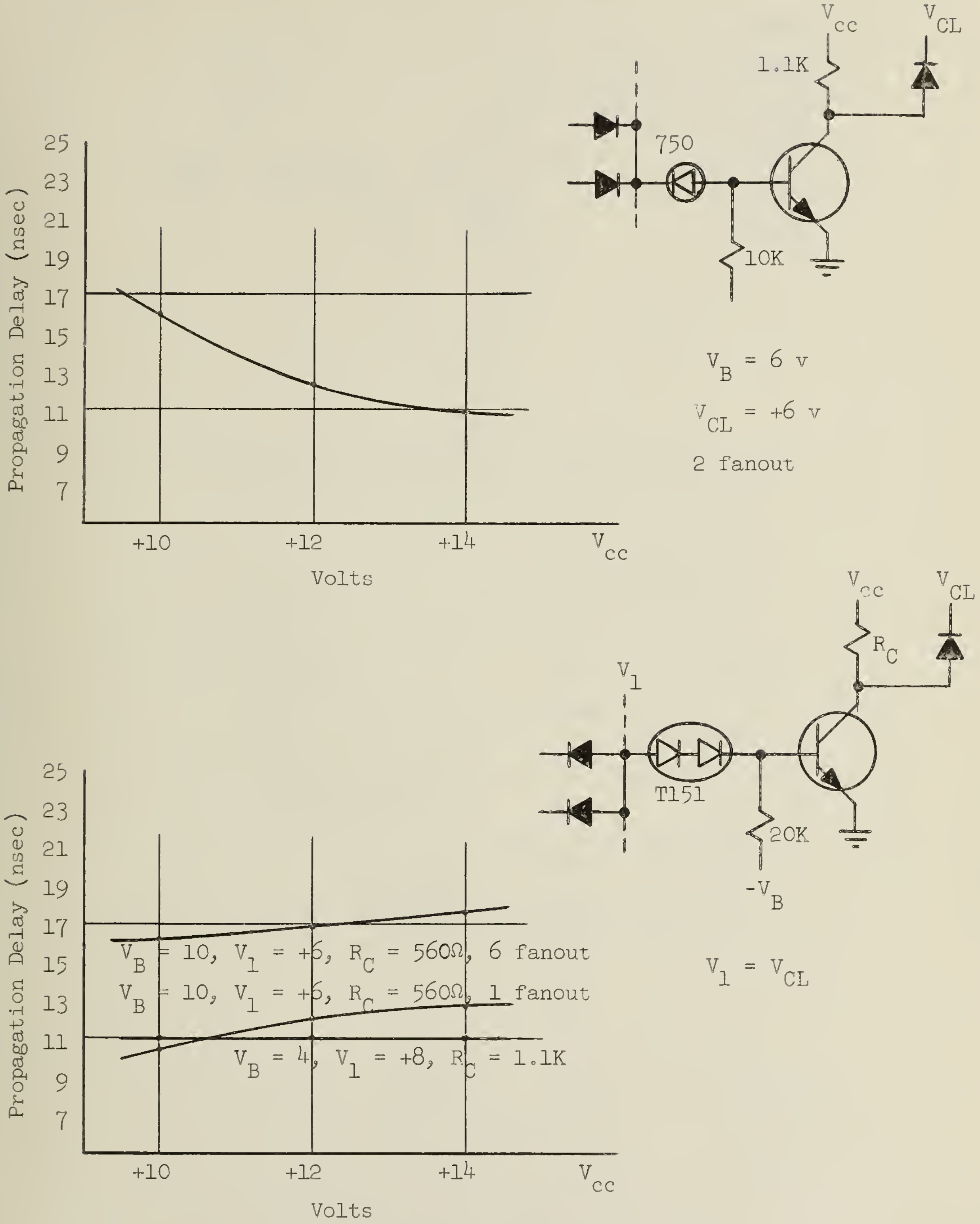


Figure 9. Propagation delay as a function of V_{CC}

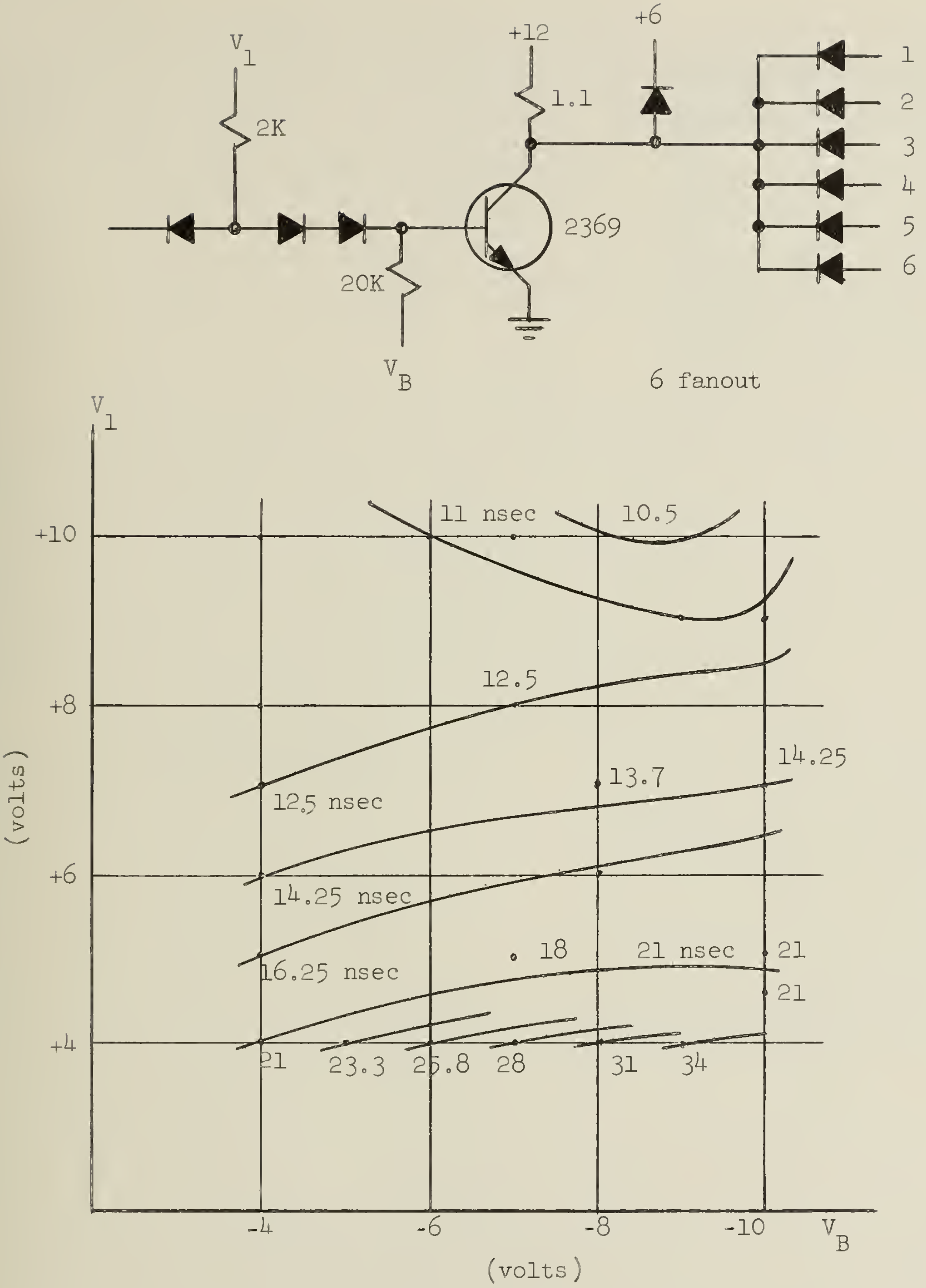


Figure 10. Equal propagation delay locus of the NAND circuit

4. COUPLING BETWEEN THE ADJACENT CIRCUITS ON THE SAME BOARD

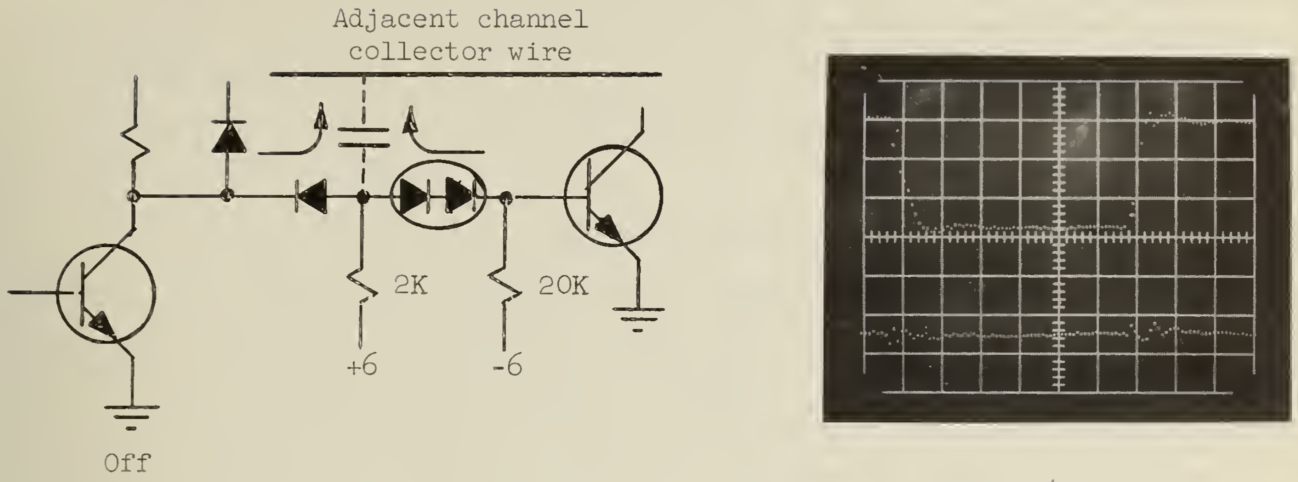
A dense arrangement of parallel circuits on one board can result in large intercircuit coupling. This coupling cannot be neglected, as it is sometimes more detrimental than the logic noise through diode capacitance.

Coupling can be calculated as follows:

$$i = \frac{d}{dt} \int_0^{\ell} C(x)V(x)dx \qquad i = \text{noise current in base circuit}$$

Figure 11 shows the data on the adjacent circuit coupling. By this measurement, the equivalent coupling in the test boards is about 3 pf. If the voltage on an adjacent collector changes at the rate of 2 v in 10 nsec, and assuming 3 pf equivalent capacitance between base and adjacent collector, this noise current can reach 0.6 ma. Therefore, to guarantee saturated operation at low temperature ($h_{FE} = 20$) with a maximum fanout of 6, we must provide approximately 2 ma for I_{b1} through the level-shifting diode (see Fig. 12 in Appendix A).

As explained in section 1, logic noise can be kept small if the collector is clamped in the NAND circuit.

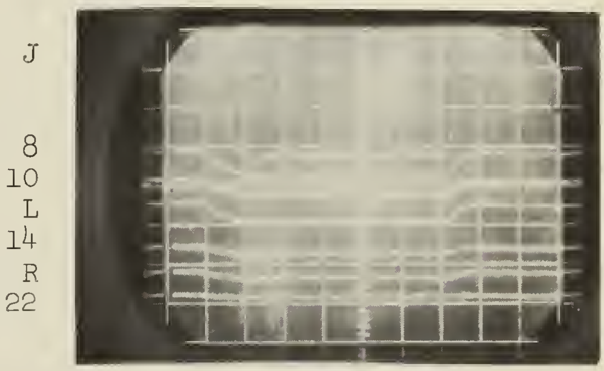


20 nsec/div
2.5 v/div

(a) Adjacent channel coupling (Equivalent capacit is 3 pf. Minimum separation of the two wires is 3/64"; average separation is approximately 1/8" along 1/2" length.)

(b) Coupling between open pin

	Distance
J-8	2/16"
J-10	5/16"
J-L	5/16"
J-14	15/16"
J-R	15/16"
J-22	2-3/16"



20 nsec/div
2.5 v/div

Figure 11

APPENDIX A: WORST-CASE EQUILIBRIUM CONDITIONS

NAND and NOR circuit design under worst-case equilibrium conditions is given here. To get an exact solution under worst-case conditions is very difficult because of the intrinsic nonlinearity of the semiconductor devices. We are unable to derive a straightforward solution, especially if the circuit has a level-shifting diode.

We are concerned with a general-purpose circuit which will be used for all logic stages without adjustment or compensation. Assuming a silicon diode and silicon transistor logic circuit, the fan-in problem will be neglected from the point of equilibrium equation. Henceforth, all transistor characteristics used for numerical evaluation are those of the 2N2369, a silicon planar epitaxial transistor. Logic diode characteristics are those of the FD100, a diffused silicon planar diode.

Table 1 shows the configuration for worst-case operation: M is the number of fan-ins, N is the number of fanouts, and transistors T_1, T_2 are as shown in Fig. 12.

Table 1. Configurations for Worst-Case Operation

NAND	T_1 off	N - 1 outputs; M - 1 inputs are all reverse biased and carry maximum leakage current	T_2 on	Lowest Temperature
	T_1 on	N - 1 outputs are forward biased and carry maximum toward current M - 1 inputs are reverse biased, maximum current flow in T_1	T_2 off	Highest Temperature
NOR	T_1 off	N - 1 outputs carry maximum forward current M - 1 are reverse biased	T_2 on	Lowest Temperature
	T_1 on	N - 1 outputs carry minimum current M - 1 inputs carry maximum current	T_2 off	Highest Temperature
	T_1 on	I_c of T_1 is maximum	T_2 on	

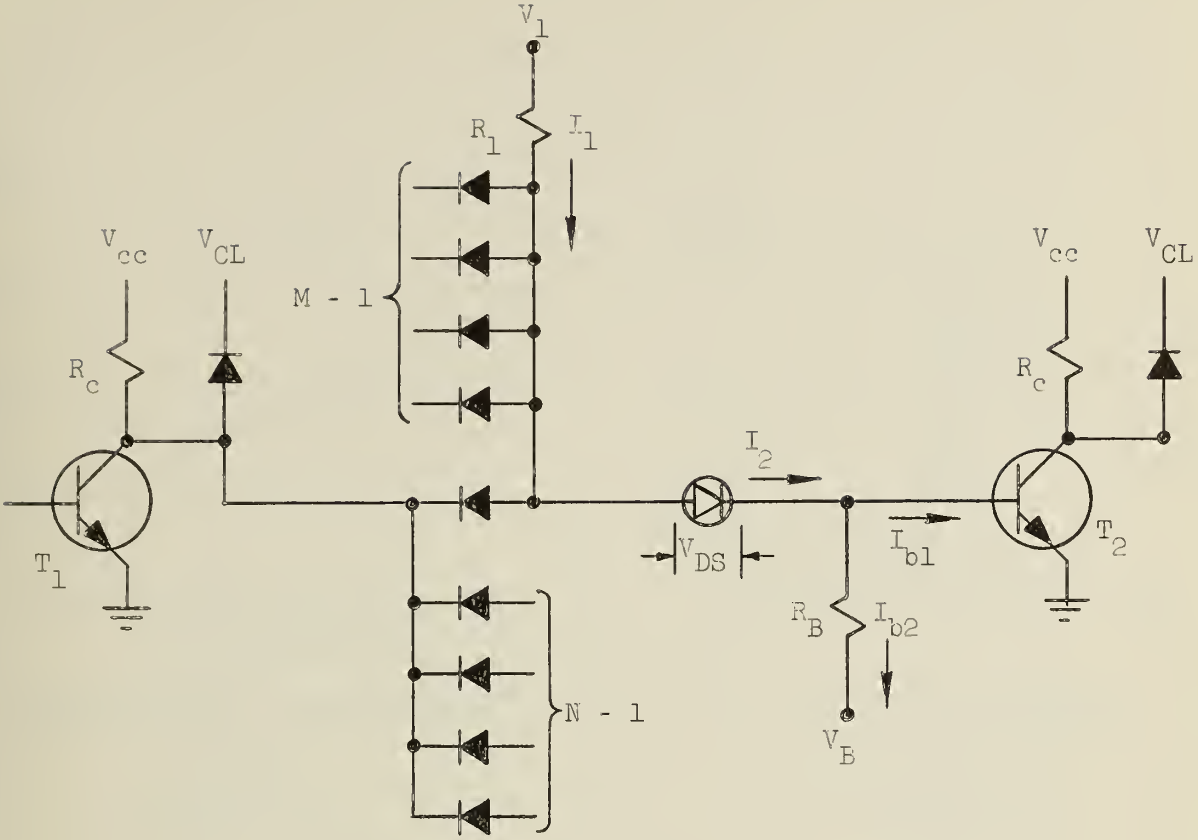


Figure 12. Configuration for worst-case operation

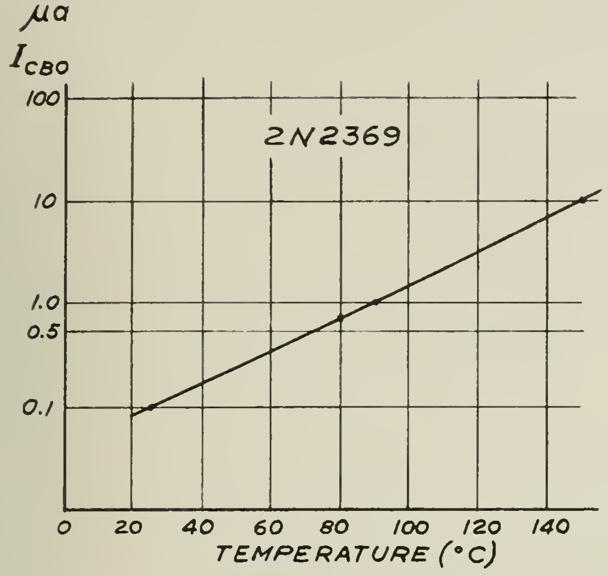
Figures 13 through 16 show how the transistor characteristics vary with temperature. As can be seen from these figures, V_{BE} decreases with increasing temperature, while V_{CE} is not linear for variation of temperature. Also the diode knee voltage decreases with increasing temperature.

The equations of the equilibrium at low temperature are:

$$\underline{I}_2 = \overline{I}_{b1} + \overline{I}_{b2} = \underline{I}_1 = \frac{\underline{V}_1 - (\overline{V}_{BE(sat)} + \overline{V}_{DS})}{\overline{R}_1} \qquad (A.1)$$

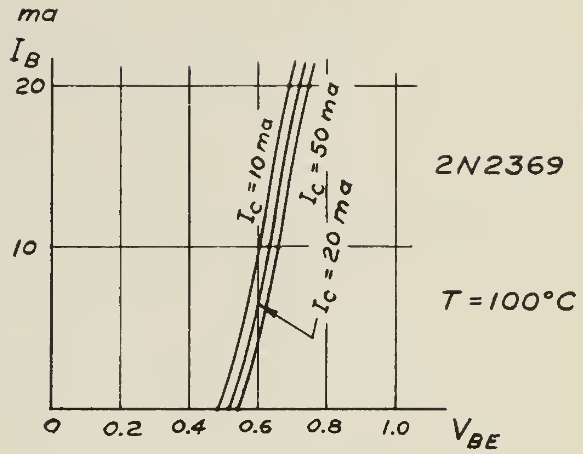
$$\overline{I}_{b1} = \frac{\overline{I}_C}{\underline{h}_{FE}} \qquad (A.2)$$

$$\overline{I}_{b2} = \frac{\overline{V}_{BE(sat)} + \overline{V}_2}{\underline{R}_B} \qquad (A.3)$$



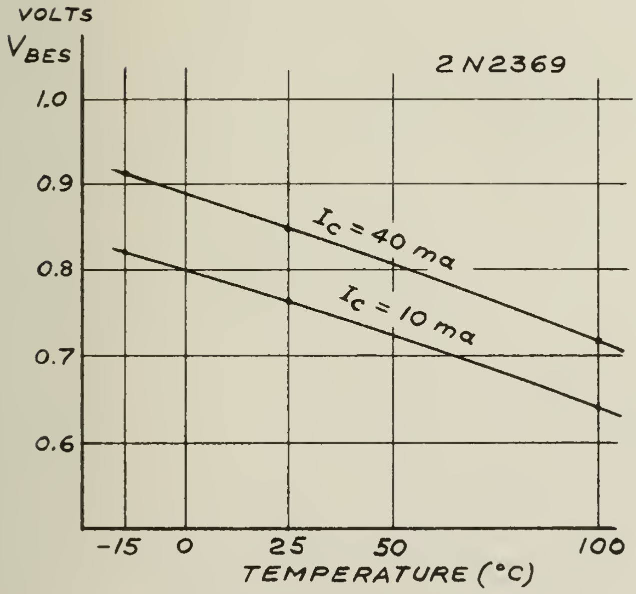
TEMPERATURE DEPENDENCE OF I_{CBO}

FIGURE 13.



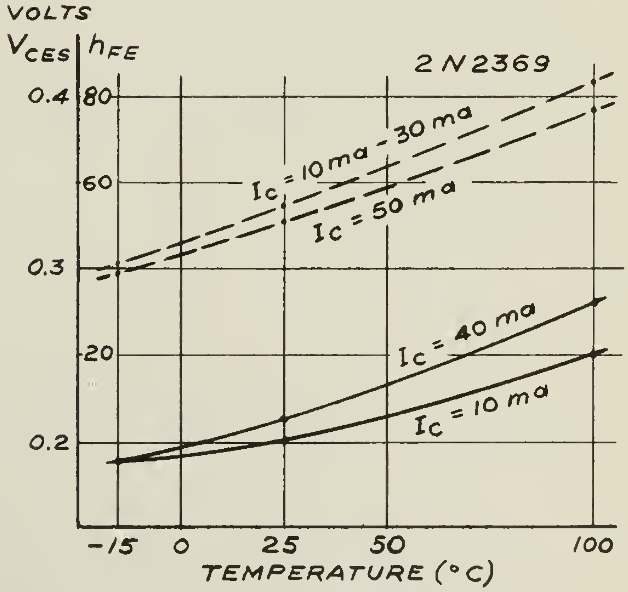
I_B VS. V_{BE} AT 100° C.

FIGURE 14.



TEMPERATURE DEPENDENCE OF V_{BES}

FIGURE 15.



TEMPERATURE DEPENDENCE OF V_{CES}

FIGURE 16.

Leakage current of the FD100 at -15°C and at a reverse voltage of 50 volts is only 13 na and at 100°C about 3 μa. Therefore even at the highest temperature, leakage current can be neglected--even when the fanout is 10.

The above equations are combined as:

$$\frac{\underline{V}_1 - (\overline{V}_{BE(sat)} + \overline{V}_{DS})}{\overline{R}_1} = \frac{\overline{I}_C}{\underline{h}_{FE}} + \frac{\overline{V}_{BE(sat)} + \overline{V}_2}{\underline{R}_B} \tag{A.4}$$

Also where $\overline{I}_c$ in Eq. (A.4) corresponds to the low temperature condition we must have:

$$\underline{V}_{cc} - \overline{R}_C \overline{I}_{EXS} > \overline{V}_{DS} + \overline{V}_{BE(sat)} + \overline{V}_D$$

At high temperature for worst-case condition, T_1 is on; T_2 is off. In this case maximum I_2 and minimum I_{b2} must guarantee the maximum V_{BEO}. Therefore the equations are:

$$\overline{I}_{b2} = \overline{I}_2 + \overline{I}_{CBO} = \frac{\overline{V}_{CEO} + \underline{V}_2}{\overline{R}_B} \tag{A.5}$$

$$\overline{I}_2 = \overline{I}_1 - \underline{I}_D = \frac{\overline{V}_1 - (\overline{V}_{CE(sat)} + \overline{V}_D)}{\underline{R}_1} - \underline{I}_D = \frac{\overline{V}_1 - (\overline{V}_{BEO} + \underline{V}_{DS})}{\underline{R}_1} - \underline{I}_D \tag{A.6}$$

These are combined to yield

$$\frac{\overline{V}_{BEO} + \underline{V}_B}{\overline{R}_B} = \left(\frac{\overline{V}_1 - (\overline{V}_{BEO} + \underline{V}_{DS})}{\underline{R}_1} - \underline{I}_D\right) + \overline{I}_{CBO} \tag{A.7}$$

Now, $\overline{I}_c$ in Eq. (A.4), is given by

$$\overline{I}_c = (N - 1)\overline{I}_D + \frac{\overline{V}_{CC} - \overline{V}_{CE(sat)}}{\underline{R}} + \underline{I}_D \tag{A.8}$$

Temperature dependence of I_{CBO} is shown in Fig. 13. From this, I_{CBO} is 3 μa at 120°C. $\underline{I}_D$ in Eq. (A.7) is a function of

$$\underline{I}_D = I_D(\overline{V}_{BEO} + \underline{V}_{DS} - \overline{V}_{CE(sat)}, \overline{V}_D)$$

and $\overline{I}_D$, $\underline{I}_D$ in Eq. (A.8). (These correspond to low temperature.)

$$\underline{I}_D = I_D(\overline{V}_{BEO} + \underline{V}_{DS} - \underline{V}_{CE(sat)}, \overline{V}_D)$$

$$\overline{I}_D = I_D(\overline{V}_{BEO} + \overline{V}_{DS} - \underline{V}_{CE(sat)}, \underline{V}_D)$$

$$\overline{V}_{DS} = (1 + \rho)V_{DS}$$

$$\underline{V}_{DS} = (1 - \rho)V_{DS}$$

$$\overline{V}_D = (1 + \eta)V_D$$

$$\underline{V}_D = (1 - \eta)V_D$$

Here parameters ρ and η designated admissible component variation, V_{DS} and V_D are threshold voltage of the level-shifting diode and logic diode respectively, and also vary with temperature. For the FD100 V_D increases eight percent at -15°C and decreasing 17 percent at +100°C. For the TI51 V_{DS} increases ten percent at -15°C and decreases 20 percent at +100°C. Therefore we can write (introducing average values $\tilde{V}_D$ and $\tilde{V}_{DS}$):

$$\overline{V}_{DS} = (1 + \rho)\tilde{V}_{DS}(1 + 0.1) \quad \text{at} \quad -15^\circ C$$

$$(1 + \rho)\tilde{V}_{DS}(1 - 0.2) \quad \text{at} \quad +100^\circ C$$

$$\underline{V}_{DS} = (1 - \rho)\tilde{V}_{DS}(1 - 0.2) \quad \text{at} \quad +100^\circ C$$

$$\underline{V}_{DS} = (1 - \rho)\tilde{V}_{DS}(1 + 0.1) \quad \text{at} \quad -15^\circ C$$

$$\overline{V}_D = (1 + \eta)\tilde{V}_D(1 - 0.17) \quad \text{at} \quad +100^\circ\text{C}$$

$$\underline{V}_D = (1 - \eta)\tilde{V}_D(1 + 0.08) \quad \text{at} \quad -15^\circ\text{C} \tag{A.9}$$

For the NOR circuit, the worst-case conditions are:

$$\underline{I}_2 = \overline{I}_{b1} + \overline{I}_{b2} = \frac{\overline{I}_C}{\underline{h}_{FE}} + \frac{\overline{V}_{BE(sat)} + \overline{V}_B}{\underline{R}_B} \tag{A.10}$$

$$\underline{V}_{CC} - \left(\overline{I}_{CEX} + (N - 1)\overline{I}_2 + \frac{\overline{I}_C}{\underline{h}_{FE}} + \frac{\overline{V}_{BE(sat)} + \overline{V}_B}{\underline{R}_B}\right)\overline{R}_C = \overline{V}_{BE(sat)} + \overline{V}_D + \overline{V}_{DS} \tag{A.11}$$

$\overline{I}_C$ is given when both T_1 and T_2 are on at low temperature by

$$\overline{I}_C = \frac{\overline{V}_{CC} - \underline{V}_{CE(sat)}}{\underline{R}_C} + N\overline{I}_{DR}$$

Here I_{DR} is the reverse current of logic diode. $\overline{I}_{DR}$ of the FD100 is again 10 μa at 100°C. Therefore this current can be neglected when the number of fanout does not exceed ten.

For high temperature the worst-case condition occurs when T_1 is on, T_2 off.

$$\overline{I}_2 + \overline{I}_{CBO} = \overline{I}_{b2} = \frac{\overline{V}_{BEO} + \underline{V}_2}{\overline{R}_B} \tag{A.12}$$

$$\overline{V}_{CE(sat)} - (\underline{V}_D + \underline{V}_{DS}) = \overline{V}_{BEO} \tag{A.13}$$

Now $\overline{I}_2$ occurs when all N - 1 outputs carry $\underline{I}_2$. (This corresponds to the case where all M - 1 inputs to T_2 are "1.")

In both NAND and NOR a certain amount of noise margin must be provided. In the case of the NAND circuit, the noise margin should be included in the $\overline{V}_{BE(sat)}$, and for the NOR included in the $\overline{V}_{BEO}$.

To solve the above equations, an iteration method is needed, but iteration is not practical except by a digital computer calculation. However a suitable choice of intermediate variables V_{DS} and I_D will make an approximate calculation possible.

From the standpoint of logic speed, V_{DS} should be small because of the delay characteristics of the NAND circuit fabricated by the 2N2369. A lower limit of V_{DS} in the NAND circuit is given by

$$\bar{V}_{CE(sat)} + \underline{V}_D - \bar{V}_{BEO} = \underline{V}_{DS}$$

at 100°C. Therefore the average value is:

$$\tilde{V}_{DS} = \frac{\bar{V}_{CE(sat)} + (1 - \eta)\tilde{V}_D(1 + 0.08) - \bar{V}_{BEO}}{(1 - \rho)(1 - 0.2)}$$

Tentatively, we have chosen the FD100 (logic) and TI51 (level shifting in NAND) diodes; forward characteristics are given in Table 2.

Table 2. Diode Forward Characteristics

	50 μa	100 μa	500 μa	1 ma	2 ma	5 ma	
$\tilde{V}_{DS}$ (TI51)	.4	.425	.453	.533	.571	.624	volts
$\tilde{V}_D$ (FD100)	.455	.49	.57	.60	.63	.70	volts

Substitute these values and $\eta = \rho = 0.2$ into the equation for $\tilde{V}_{DS}$; we get

Min $\tilde{V}_{DS}$ =			
0.77	for $V_{BEO} = 0.3$	$\bar{V}_{CE(sat)} = 0.3$	$I_{DS} = 500$ μa
0.81	for $V_{BEO} = 0.3$	$\bar{V}_{CE(sat)} = 0.3$	$I_{DS} = 1$ ma
0.85	for $V_{BEO} = 0.3$	$\bar{V}_{CE(sat)} = 0.3$	$I_{DS} = 2$ ma

Therefore to guarantee operation at 100°C under the 20-percent variation in the forward voltage drop of the level-shifting diode, we require two silicon diodes in series for level shifting.

Due to variations in temperature and diode characteristics, $\underline{I}_D$ and $\overline{I}_D$ are related as follows:

$$\underline{I}_D \text{ (in Eq. (A.8))} = \underline{I}_D \text{ (in Eq. (A.7))} \ (1 - 0.17)(1 - 0.08)$$

$$\overline{I}_D \text{ (in Eq. (A.8))} = \underline{I}_D \text{ (in Eq. (A.7))} \ (1 + \eta)(1 - \rho)(1 - 0.17)(1 - 0.08)$$

Therefore $\overline{I}_C$ is now expressed as:

$$\overline{I}_C = (N - 1)(1 + \eta)(1 - \rho)\underline{I}_D(1 - 0.17)(1 - 0.08) + \frac{\overline{V}_{CC} - \underline{V}_{CE(sat)}}{\underline{R}_C} + \underline{I}_D(1 - 0.17)(1 - 0.08)$$

For the NOR circuit, similar relations hold, but it would be redundant to described all of them. Numerical calculations are given only for the NAND circuit for the same reason.

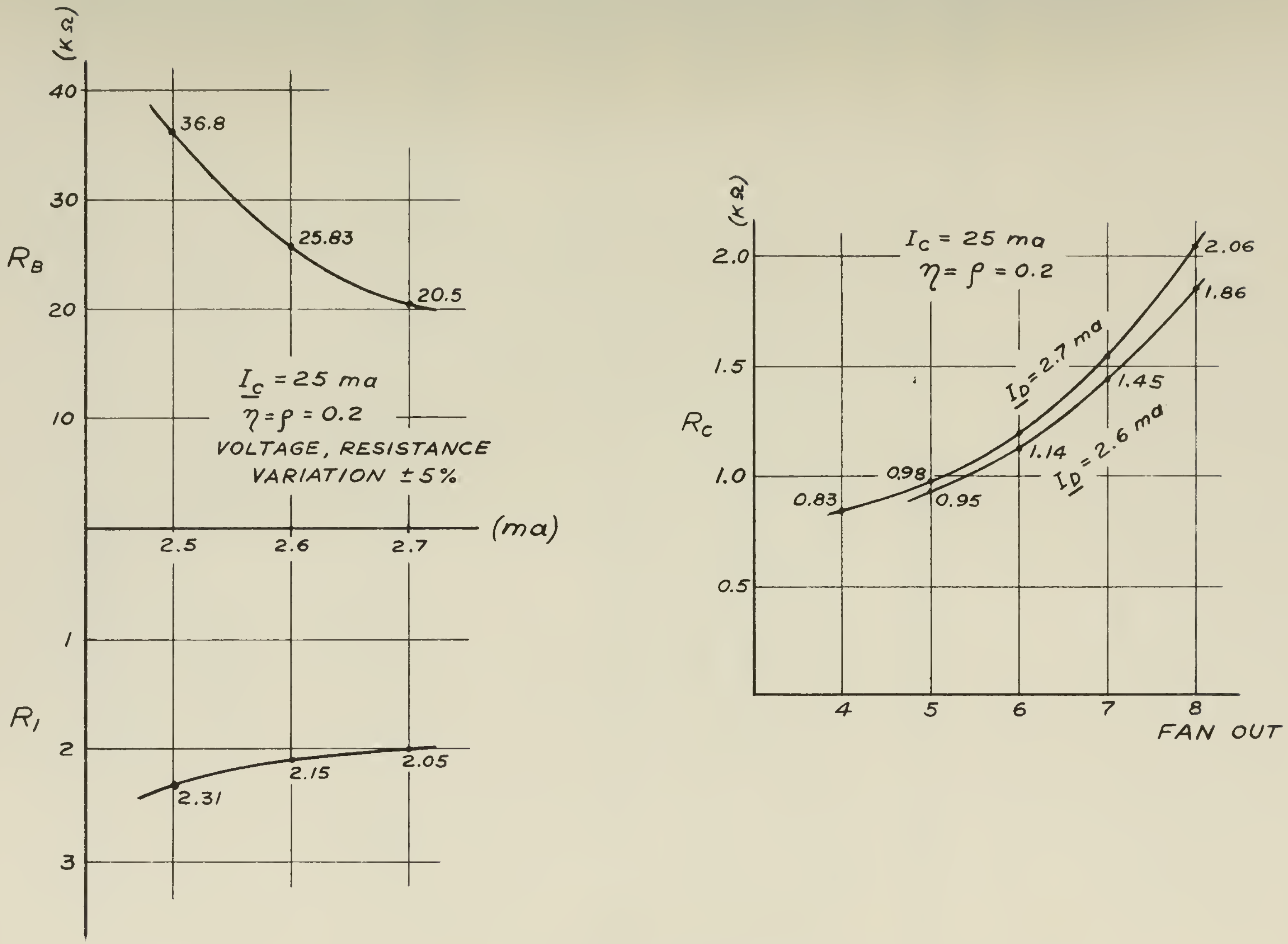
The 2N2369 has the following static characteristics:

$\overline{V}_{BE(sat)}$	at	-15°C	0.9 volts	
$\underline{h}_{FE}$	at	-15°C	20	
$\overline{V}_{BEO}$	at	+100°C	+0.3 volts	
$\underline{V}_{CE(sat)}$	at	-15°C	0.2 volts	(I_C = 10 ma ~ 40 ma)
$\overline{V}_{CE(sat)}$	at	+100°C	0.3 volts	(I_C = 10 ma ~ 40 ma)
$\overline{I}_{CBO}$	at	+100°C	3 μa	
$\Delta V_F/^\circ C$	for the FD100		-1.8 mv	

The solution of the equations for the given variation of components, voltage, and temperature range is determined for the given values of the intermediate variables, I_C, N, $\underline{I}_D$, V_{DS}. For the calculations, variation of diode

characteristics is assumed to be ± 20 percent; resistance variation is 5 percent; and the temperature range is -15°C to +100°C. In the numerical calculations, $\bar{V}_{BEO}$ at +100°C was taken as 0 volt, and $\bar{V}_{BE(sat)}$ at -15°C was taken as +1.0 volts.

From Eqs. (A.4), (A.7), (A.9), (A.14), we get the solution shown in Fig. 17.



THE CALCULATED VALUE OF THE NAND CIRCUIT COMPONENTS.

FIGURE 17.

APPENDIX B: SWITCHING WAVEFORMS

Switching performance of the transistors (2N2369) themselves are very uniform. But when fabricated into logic circuits (because of the nonlinear transients and difficulty of solving the resulting equations) it is difficult to estimate the switching waveform. However even approximate waveform considerations can give much help in the design of the circuit. An approximate description of the waveform will be given in this Appendix. Switching speed of the circuit in most networks is also limited by coupling between conductors, parasitic capacitance and inductance.

Turn-on Waveform

The turn-on waveform of the circuit with fanout is principally composed of two parts, as shown in Fig. 18.

Increasing the number of fanouts gives only a small change in turn-on time because of the nonlinearity of h_{FE} $\frac{\partial h_{FE}}{\partial I_c} > 0$ and the small output resistance of the transistor. For both NAND and NOR, after the input diode of the next stage changes, build-up speed of the present stage generally decreases.

The capacitive coupling between base and collector acts as an integrator; therefore, even if the transistor has infinite speed, the build-up time constant is βCR_B.

Turn-off Waveform

The typical waveform, shown in Fig. 18, is more complicated than the turn-on waveform. For the first period of turn-off, the waveform is approximated by

$$\frac{r(t)V_{cc}}{R_c + r(t)}\left[1 - \frac{r(t)}{R_1}\right], \qquad \text{if } r(t)C \ll 1 \qquad \text{(B.1)}$$

Here r(t) is the output resistance transient characteristic. In this period, the effect of load capacitance is negligible because the transistor is still in the active region.

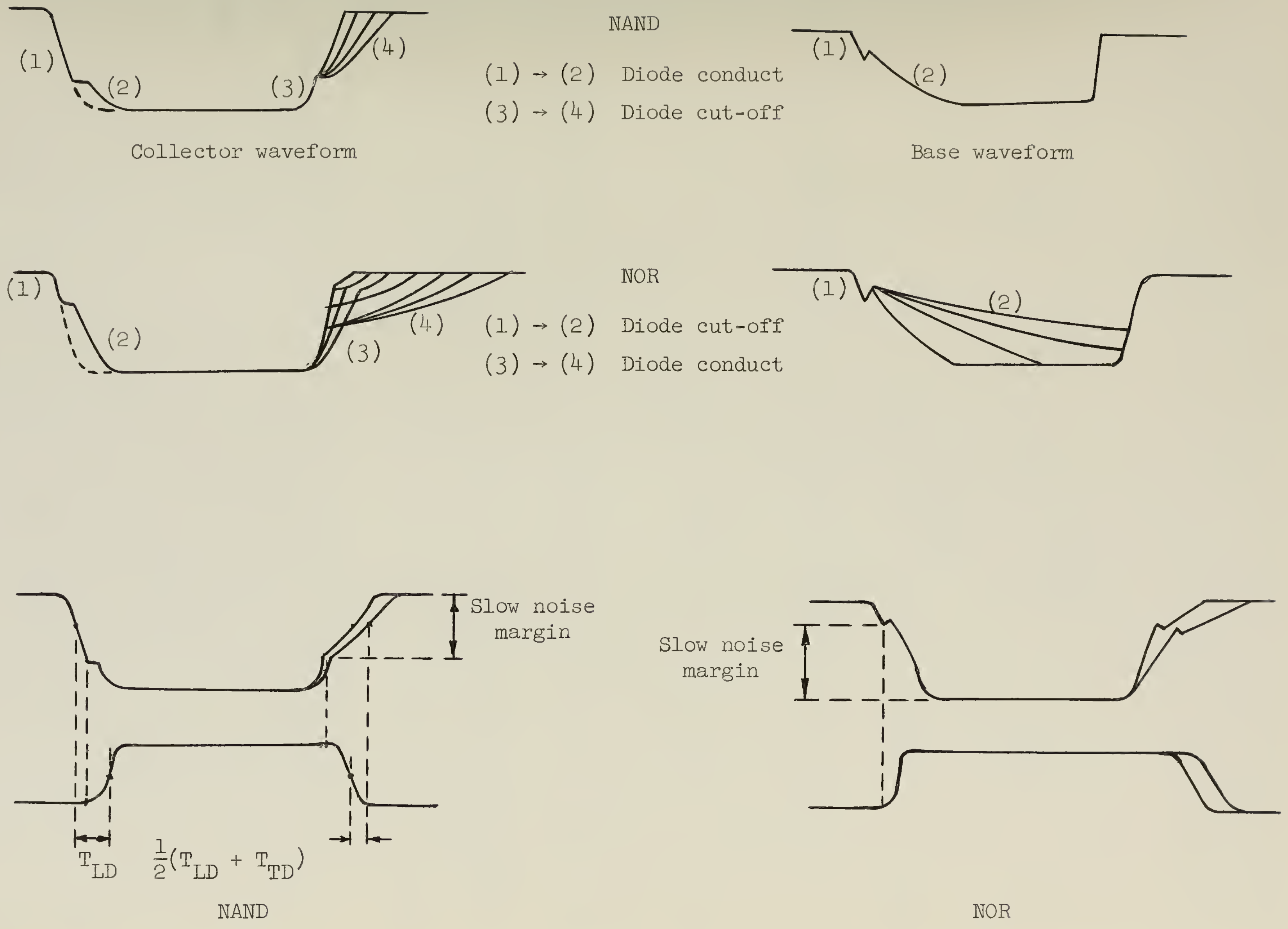

(1)
(2)
(3)
(4)
Collector waveform
NAND
(1) → (2) Diode conduct
(3) → (4) Diode cut-off
(1)
(2)
Base waveform
(1)
(2)
(3)
(4)
NOR
(1) → (2) Diode cut-off
(3) → (4) Diode conduct
(1)
(2)
Slow noise margin
T_{LD}
$\frac{1}{2}(T_{LD} + T_{TD})$
NAND
Slow noise margin
NOR

Figure 18

Passing through this period, turn-off characteristics are determined by the load capacitance and load resistance (for NAND, also by bias resistance). The waveform here is approximated by (until the disconnection of the next stage input diode):

$$V_{cc}\left(1 - e^{-\frac{t}{R_c C}}\right) + V_1\left(1 - e^{-\frac{t}{R_1 C}}\right) \qquad \text{for NAND} \qquad (B.2)$$

$$V_{cc}\left(1 - e^{-\frac{t}{R_C C}}\right) \qquad \text{for NOR} \qquad (B.3)$$

After disconnection of the next stage input diode, the waveform is:

$$V_{cc}\left(1 - e^{-\frac{t}{R_c C}}\right) \qquad \text{for NAND} \qquad (B.4)$$

until clamping sets in. The cutoff clamping level is determined by the clamping diode in the NAND, and by the $V_{BE(sat)}$ in the NOR.

From the above behavior, to reduce propagation delay, the conducting level should be chosen to occur in the range of $r(t)C \ll 1$. If designed according to this criterion, propagation delay does not depend upon the number of fanouts.

For the NOR circuit, however, to specify the conducting level as described above would decrease the high-frequency noise margin. Therefore this design cannot be applied. For the NOR circuit, the turn-off waveform, to be compared with the NAND waveform, is also shown in Fig. 18. The waveform, after the input diode of the stage (NOR) reaches conduction, is the charging curve of the level-shifting diode capacitance. Therefore the time constant depends on the negative base bias level. When this negative level is low, the charging time constant is smaller and the conducting level of the input diode is higher--if the next turn-on signal arrives fast. This situation can be easily understood by referring to the base waveform in Fig. 18. The main difference in the turn-off characteristics of the NAND and the NOR comes from the change in conduction of the level-shifting diode in the base circuit. The higher conduction

level always results in more delay for propagation. Therefore we must take into account the above situation when determining the negative bias voltage.

Noise Margin

Noise margins of the NAND and NOR are also indicated in Fig. 18. This margin has different values for slow noise than for the fast noise.

For slow noise, the margin is equal to the difference between the clamp level and the conducting level for the NAND, and equal to the difference between $V_{CE(sat)}$ and conducting level for the NOR. For high-frequency noise, this margin is referred to $V_{BE(sat)}$ in the NAND, and to V_{BEO} in the NOR. Noise can sometimes cause considerable delay until the waveform recovers to the correct value. This is the one disadvantage of saturated operation.

The delay per logic function is shown also in Fig. 18. This delay is more sensitive to fanout for the NOR than for the NAND because the delay depends mostly upon turn-on for the NAND circuit and upon turn-off for the NOR circuit.